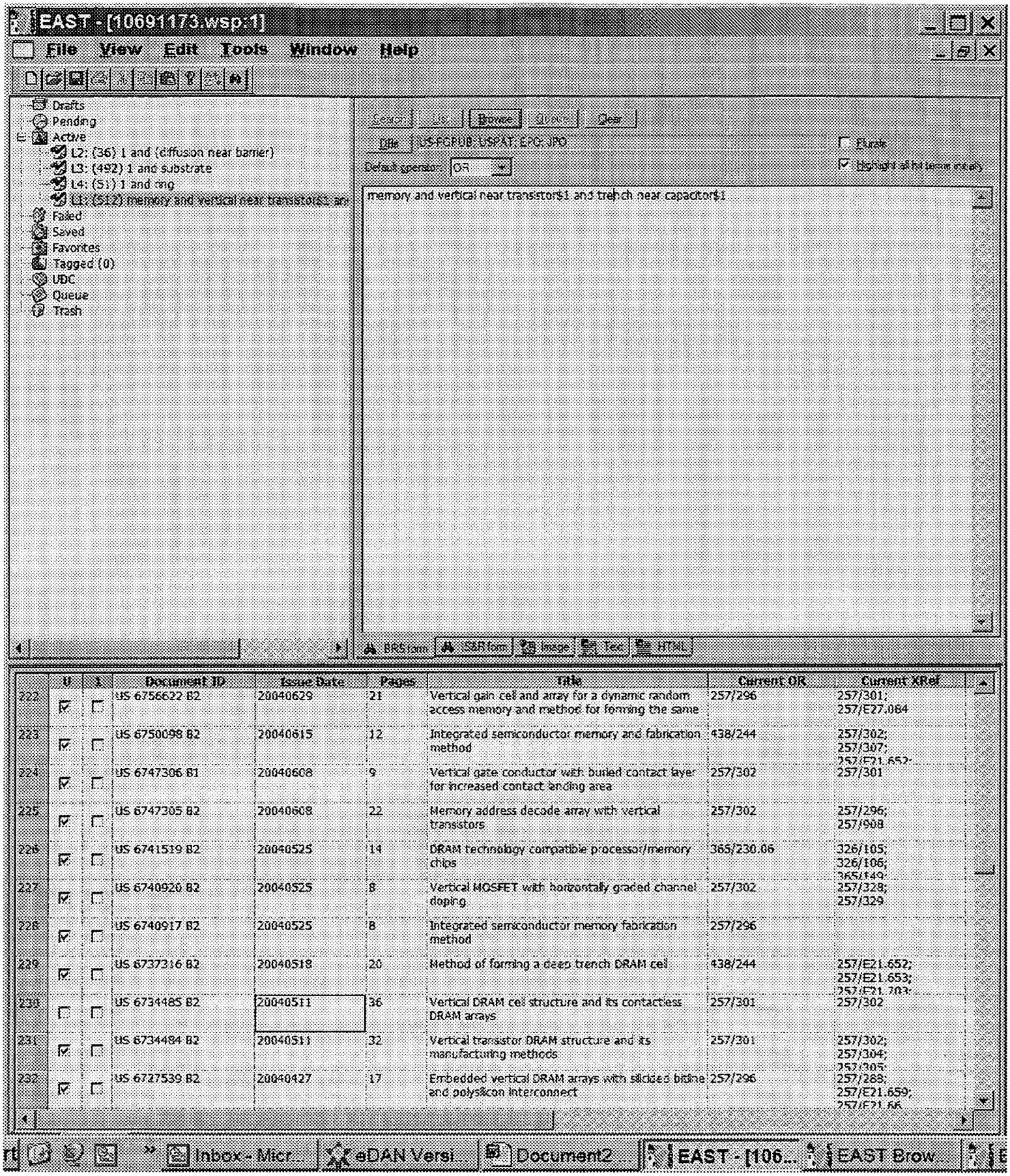
EAST - [10691173.wsp:1]
File View Edit Tools Window Help
Drafts
Pending
Active
L2: (36) 1 and (diffusion near barrier)
L3: (492) 1 and substrate
L4: (51) 1 and ring
L1: (512) memory and vertical near transistor$1 an
Failed
Saved
Favorites
Tagged (0)
UDC
Queue
Trash
Search
Clear
Browse
Clear
Diff
US-PGPUB; USPAT; EPO; JPO
Plural
Highlight all hit terms initially
Default operator: OR
memory and vertical near transistor$1 and trench near capacitor$1
BRS form
ISR form
Image
Tec
HTML
U
1
Document ID
Issue Date
Pages
Title
Current OR
Current XRef
222 US 6756622 B2 20040629 21 Vertical gain cell and array for a dynamic random access memory and method for forming the same 257/296 257/301; 257/E27.084
223 US 6750098 B2 20040615 12 Integrated semiconductor memory and fabrication method 438/244 257/302; 257/307;
224 US 6747306 B1 20040608 9 Vertical gate conductor with buried contact layer for increased contact landing area 257/302 257/301
225 US 6747305 B2 20040608 22 Memory address decode array with vertical transistors 257/302 257/296; 257/908
226 US 6741519 B2 20040525 14 DRAM technology compatible processor/memory chips 365/230.06 326/105; 326/106;
227 US 6740928 B2 20040525 8 Vertical MOSFET with horizontally graded channel doping 257/302 257/328; 257/329
228 US 6740917 B2 20040525 8 Integrated semiconductor memory fabrication method 257/296
229 US 6737316 B2 20040518 20 Method of forming a deep trench DRAM cel 438/244 257/E21.652; 257/E21.653;
230 US 6734485 B2 20040511 36 Vertical DRAM cell structure and its contactless DRAM arrays 257/301 257/302
231 US 6734484 B2 20040511 32 Vertical transistor DRAM structure and its manufacturing methods 257/301 257/302; 257/304;
232 US 6727539 B2 20040427 17 Embedded vertical DRAM arrays with silicided bitline and poly&con interconnect 257/296 257/288; 257/E21.659;
Inbox - Micr...
eDAN Versi...
Document2 ...
EAST - [106...
EAST Brow...